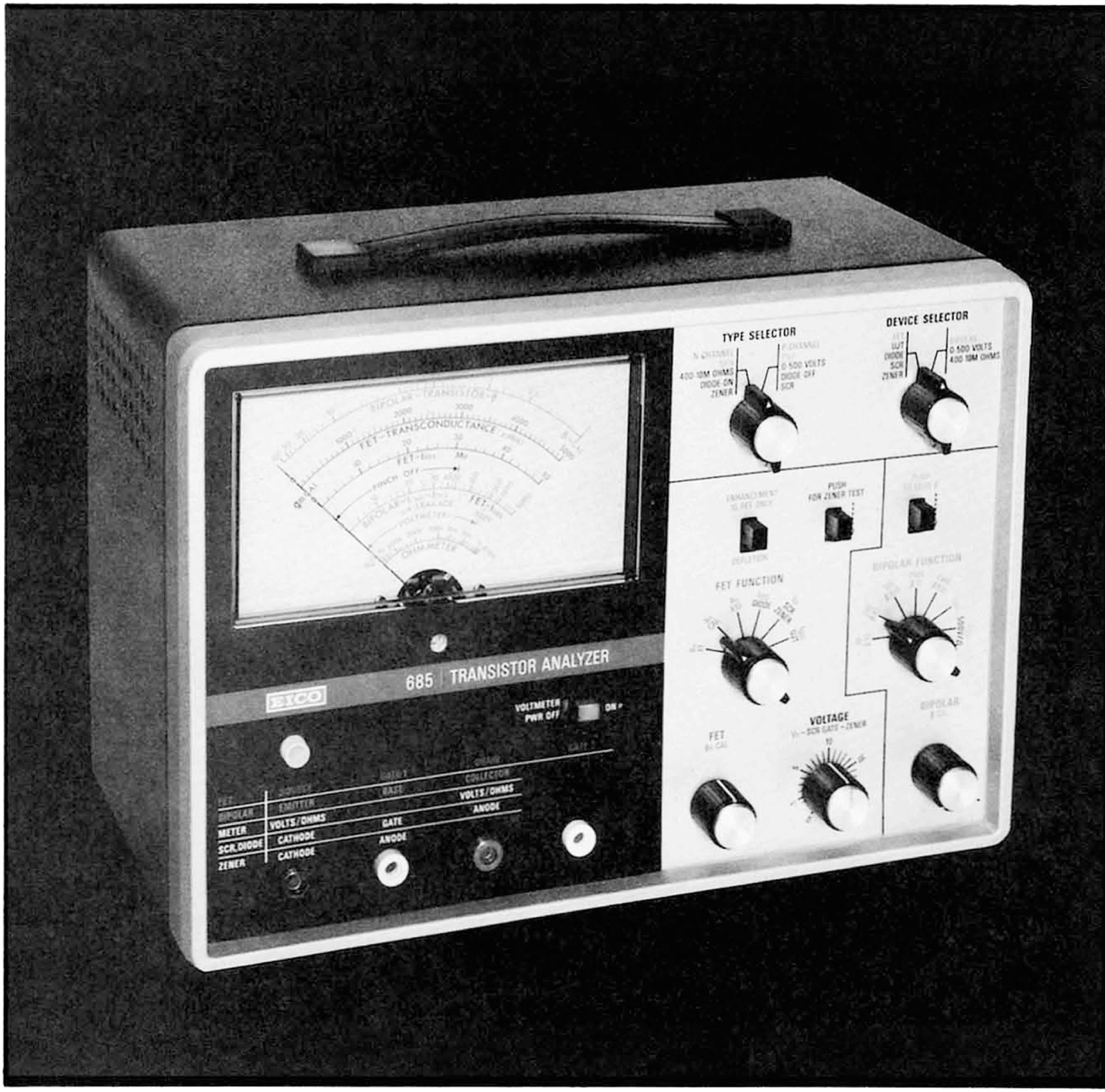
EICO®

685 | Transistor Analyzer



OPERATING MANUAL

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GENERAL DESCRIPTION

The EICO Model 685 Dynamic Semiconductor and Circuit Analyzer is a "state of the art" instrument that tests bipolar transistors and field effect transistors (FET's) both in and out of circuit. It can also be used to test UJT's, SCR's, and many types of diodes. In addition, an accurate voltmeter and ohmmeter are integral parts of the Model 685. This tester has been designed to fulfill the technician's requirements of convenience and speed while satisfying the engineer's need for accuracy and versatility.

FEATURES

1. For bipolar transistors, checks power, signal and critical RF types in or out of circuit, reading a-c beta accurately. Measurement of leakage currents I_{CBO}, I_{CEO}, and I_{CES} can be made, with the results displayed on an accurate compressed meter scale.

2. FET's can be checked for a-c transconductance (g_m), as well as gate leakage (I_{GSS}), zero bias drain current (I_{DSS}), and pinch-off voltage (V_p). Both enhancement and depletion devices can be checked with equal ease and with equally accurate results.

3. The versatility of the instrument permits its use in performing significant tests on other semiconductor devices such as unijunction transistors, controlled rectifiers, power rectifiers, signal diodes, and zener diodes.

4. A built-in d-c voltmeter and ohmmeter, using a single knob setting, permits convenient testing of the circuit that contains the semiconductor being checked.

5. A 50-microampere 6" Taut Band meter used in combination with close tolerance (1%) resistors, ensures accurate readings and provides sufficient sensitivity to obtain meaningful leakage measurements.

SPECIFICATIONS

Bipolar Transistor Tests

AC Beta (in and out of circuit):	2-100 (readings to 1000) at I_c = 0.2 ma for RF devices
	2-100 and 2-1000 (readings to 10,000) at I_c = 2 ma for small signal devices
	2-100 and 2-1000 (readings to 10,000) at I_c = 20 ma for power devices
I_{CBO}:	0-5 ma
I_{CEO}:	0-5 ma
I_{CES}:	0-5 ma

FET Tests

AC Transconductance (g_m)(in and out of circuit):	0-5000 and 0-50,000 micromhos at V_{DS} = 5v and V_{GS} = 0
I_{DSS}:	0-50 ma (linear scale)
I_{GSS}:	0-5 ma
V_p:	0-20v at V_{DS} = 5v

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UJT Test:	Establishes condition of device
SCR and Triac Test:	Establishes condition of device and indicates gate turn-on voltage
Signal Diode and Rectifier Test:	Establishes condition of device from forward and reverse current tests.
Zener Diode Test:	Establishes condition of device and indicates zener breakdown voltage
Voltmeter:	0-500 volts (30 volts center scale), 1 megohm resistance
Ohmmeter:	400 ohms to 10 megohms (130 kilohms center scale).
Semiconductor Complement:	2 - 2N5172 1 - 1N3600 (selected) 1 - 1N662 2 - 1N34 5 - 100 PIV, 500 ma rectifiers 1 - 6.8-volt zener 1 - 9.1-volt zener 1 - 24-volt zener
Meter Movement:	50 μa 2% Taut Band
Power Requirements:	105-132 volts, 50/60 Hz, 10 watts
Size:	12-1/2" high, 8-1/2" wide, 6" deep
Weight:	10 pounds

TRANSISTOR BASICS

General. The following paragraphs will provide the user of the EICO Model 685 with useful transistor background information. Familiarity with this information will help the technician to make meaningful use of this instrument. For a more comprehensive description of the subject, the reader is referred to Howard W. Sams & Co. publication No. 20659, "Practical Design with Transistors."

Terminology. Since the Model 685 checks many parameters of both bipolar and FET type transistors, the user of this instrument should be familiar with the terms employed. The terminals of a bipolar transistor are designated C (collector), B (base), and E (emitter). In a field effect transistor (FET), the terminals are D (drain), G (gate), and S (source). By using these abbreviations as subletters, various terms can be designated. For example, bipolar transistor term I_{CBO} represents the leakage current flow between collector (C) and base (B), with the O indicating that the third element, the emitter (E) in this case, is open. Similarly, the bipolar transistor term I_{CEO} stands for the leakage current flow between collector and emitter, with the base open.

The terms I_{DSS} and I_{GSS} are used with FET's. I_{DSS} represents the current flow from drain (D) to source (S). The third subletter, S, indicates that the second element (the source) is shorted to the third element (the gate) so that zero bias exists. Thus, I_{DSS} is termed the zero bias drain current. I_{GSS} is gate-to-source leakage current. In this case, the second element (the source) is shorted to the third element (the drain).

Bipolar Transistor Tests. The Model 685 is designed to measure a-c beta, I_{CBO}, and I_{CEO} of bipolar transistors. Beta, represented by the Greek letter β , is the current amplification factor. It is the rate of change in the collector current divided by the change in the base current while maintaining the collector-emitter voltage constant. The range of β values varies with transistor types. The Model 685 provides five scales for measuring the β of r-f, signal, and power transistors.

I_{CBO}, the leakage current that flows between base and collector, is another significant parameter that can be measured. Leakage current is especially critical in circuits where large temperature variations are encountered, since the leakage current increases when the temperature rises.

I_{CEO}, collector-to-emitter leakage current with the base lead open, is another bipolar transistor parameter of interest. Transistors characterized by excessive values of leakage current I_{CEO} are undesirable for many applications. I_{CES}, collector-to-emitter current with the base lead connected to the emitter, can also be measured.

FET's. The FET is somewhat similar to the vacuum tube in that the input terminal (gate) is reverse biased and the output (drain) current depends upon the gate voltage. Characterized by a high-impedance input, the gain of an FET is a function of its transconductance (g_m). Its characteristic curves resemble those of pentode vacuum tubes. The two basic FET types are the junction FET (JFET) and the metal-oxide semiconductor gate FET (MOSFET). The latter is also known as the insulated gate FET (IGFET). Both devices may have either a P-channel or an N-channel.

Three modes of operation are associated with FET's: the depletion mode, the enhancement mode, and the depletion-enhancement mode. JFET's operate in the depletion mode; i.e., drain current flows even in the absence of a gate-to-source voltage, V_{GS}. For the N-channel JFET, a negative gate voltage lowers channel conduction. A positive gate voltage has a similar effect on the P-channel JFET. The amount of voltage required to reduce channel conduction to zero is called the pinch-off voltage, V_p.

Only IGFET's are used as enhancement devices. Here, zero bias cuts off drain current. For N-channel FET's, drain current increases as V_{GS} is made more positive. In P-channel FET's, more negative values of V_{GS} cause drain current to increase. IGFET's are made in both the enhancement and depletion types. An ENHANCEMENT-DEPLETION switch on the Model 685 selects the proper bias for the type of FET to be tested.

FET Tests. The Model 685 provides readings of ac transconductance (g_m) as well as I_{DSS}, I_{GSS}, and pinch-off voltage. I_{DSS} is zero bias drain current. I_{GSS} is gate leakage current. These four tests represent the most significant FET parameters. When used in balanced circuits, FET's must be carefully matched for g_m.

CIRCUIT DESCRIPTION

The following paragraphs provide a brief description of the circuits used when each of its various test functions is being performed by the Model 685. In each case, a simplified schematic diagram of the circuit is presented as an aid to understanding the associated description. For purposes of simplification, N-channel FET's and NPN transistors are described in the text. However, the drawings also show the circuit variations for testing P-channel FET's and PNP transistors.

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a. <u>FET g_m Calibration</u> (See figures 1A and 1B.)

In general, the upper winding of T1 develops the basic drain voltage required for testing FET's while the bottom winding performs a similar function for the FET gate. The a-c voltage developed across the upper winding performs a second function. In conjunction with diodes D1 and D2, it provides a full-wave rectified voltage that is filtered by R3 and C1. A constant +6.8-volt level is developed across zener diode D5. This d-c voltage serves as the collector supply for balance transistors Q1 and Q2. It is also divided down by R4 and R5 for use in other circuits of the Model 685.

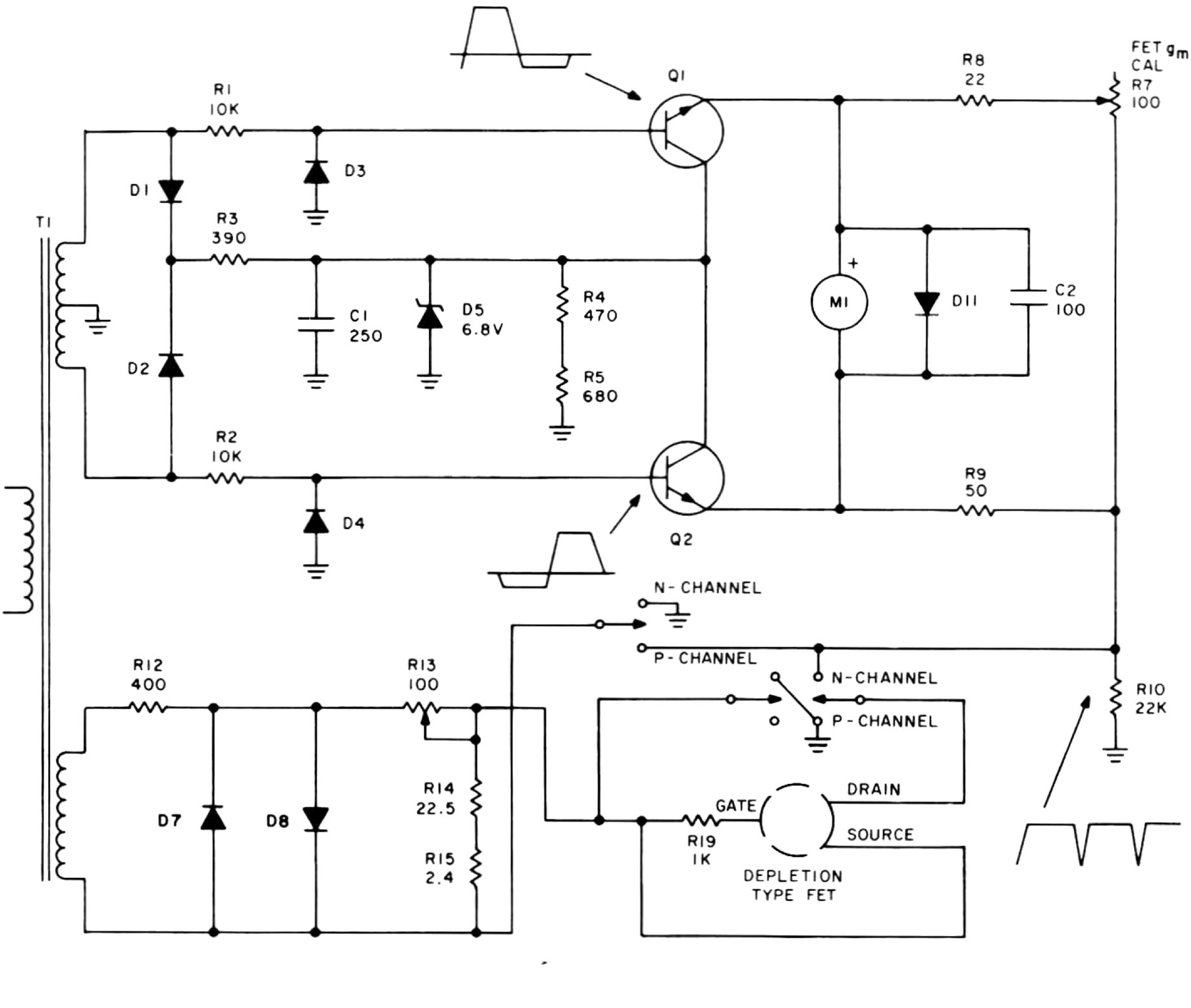

Figure 1A. g_m CAL Circuit, Depletion Mode FET

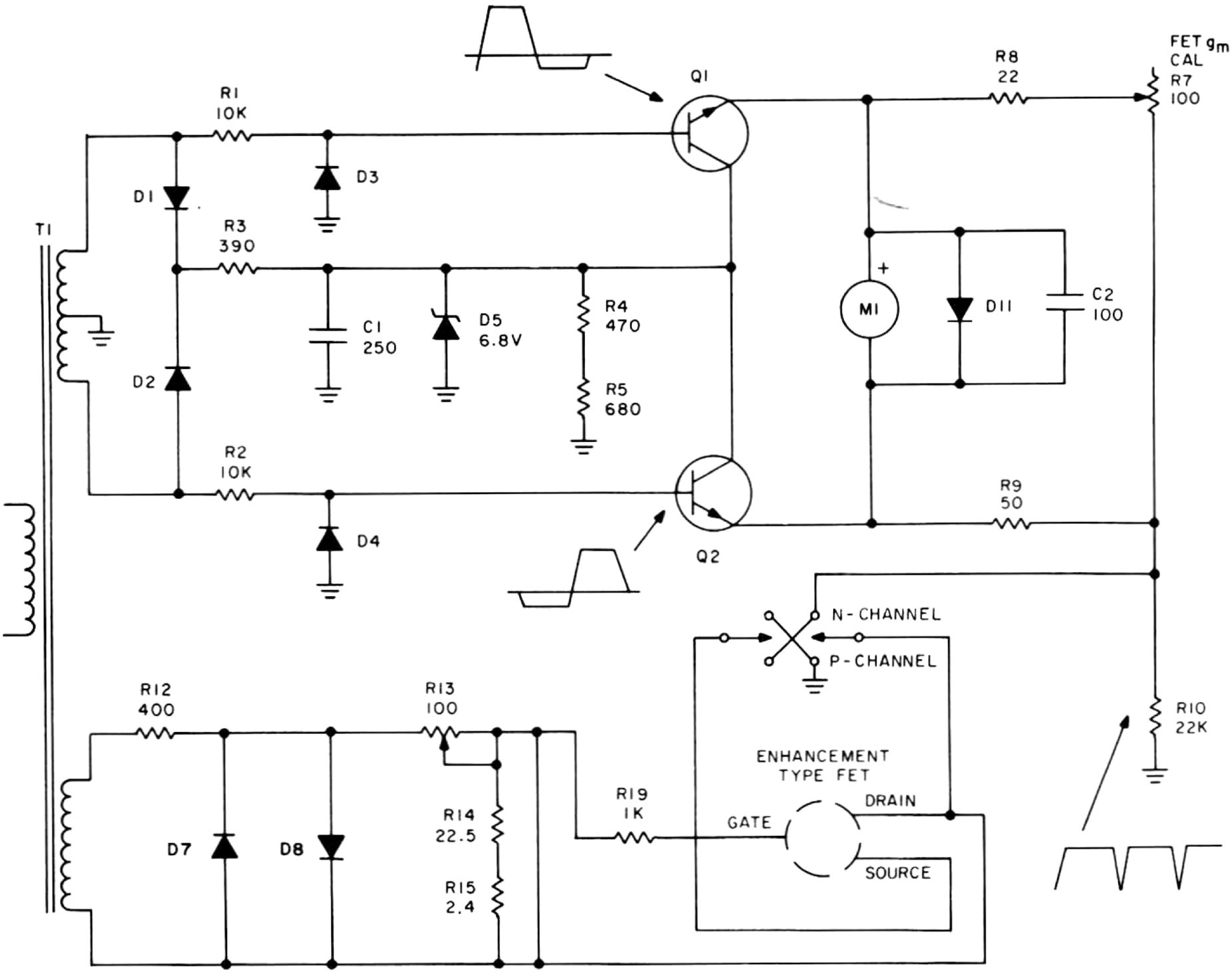

Figure 1B. g_m CAL Circuit, Enhancement Mode FET

Diodes D3 and D4, in conjunction with resistors R1 and R2, clip the negative-going voltage excursions supplied by the same transformer winding. The waveform at the base of each transistor is developed as follows: When the a-c input is positive going, that transistor is forced into saturation. At saturation, the collector-to-base voltage drops to a low value. This causes the base voltage to rise almost to the 6.8 collector voltage, producing the positive portion of the waveform shown at the base. When the a-c input goes negative at the end of the first half-cycle, it forward biases the diodes connected at the bases, clipping the a-c voltage at about 0.2 volt. (The 0.2 volt is the negative portion of the waveform shown.) The associated transistor is turned off as a result of the low base voltage. Thus, Q1 and Q2 conduct on alternate half cycles, switching on and off.

When Q1 conducts, its collector current passes through M1 in series with R9 (the combination of which is shunted by R7 and R8) and then through series resistor R10. When Q2 conducts, it causes current to flow through the series combination of M1, R8, and R7, shunt-connected R9, and series resistor R10. In this case, the direction of current flow through M1 is reversed. Since the value of R10 is much higher than the other resistors, most of the voltage developed at the emitters of Q1 and Q2 appears across R10, producing the waveform shown. This constitutes the drain voltage supply for the FET under test.

When the front panel FET FUNCTION switch is set to the g_m CAL position and a depletion mode FET is being tested, the gate of the FET under test is shorted to the source via R19 (figure 1A). For enhancement mode FET's, the gate is similarly shorted to the drain via R19 (figure 1B). Therefore, the drain current of the FET is controlled mainly by the drain voltage pulses applied from the Q1-Q2 switching circuit. The FET g_m CAL control R7, is adjusted so that equal currents flow through the meter on alternate half cycles. Since equal current flows in both directions, when adjusted, balancing the circuit produces a zero meter reading. This calibrates the FET g_m circuit.

N-channel or P-channel FET's operating in either the depletion or enhancement mode can be calibrated for test. The switching circuits in the Model 685 set up the proper polarities and voltages for the particular type selected, as shown.

b. <u>FET g_m X 1 Operation.</u>

When the FET FUNCTION switch is set to the g_m X1 position, the circuit assumes the form shown in figures 2A and 2B. At this time, a constant amplitude (0.4 volt peak-to-peak) square wave developed across R14 and R15 is applied to the gate of the FET under test. The square wave is derived from the lower winding of transformer T1. The combination of diodes D7 and D8 in series with R12 clips the a-c waveform, which then appears across R13, R14, and R15. Potentiometer R13 is adjusted so that precisely 0.4 volt peak-to-peak is developed across R14 and R15.

When the square wave signal is fed to the gate of the FET being tested, it causes the FET to conduct more heavily on one half of the cycle than the other. Current flow through the meter then becomes unequal, producing a meter reading. The signal polarity is arranged so that meter current in the forward direction exceeds the meter current in the reverse direction for the particular FET under test, producing a normal up-direction meter deflection. Since $g_m = \frac{\Delta I_D}{\Delta V_G}$ and ΔV_G is maintained constant, the meter reading produced by the change in drain current is proportional to the g_m of the FET and is calibrated accordingly (0-5000 μ mhos).

c. <u>FET g_m X 10.</u>

When the FET FUNCTION switch is set to the g_m X10 position, the voltage applied to the gate of the FET under test is reduced from 0.4 volt to 0.04 volt peak-to-peak. Since $g_m = \frac{\Delta I_D}{\Delta V_G}$ and the constant ΔV_G is 1/10 the value used for the g_m X1 measurement, the meter reading becomes g_m X10, providing a maximum reading of 50,000 μ mhos.

d. <u>Measurement of I_{DSS}.</u> (See figure 3.)

When measuring I_{DSS} (zero bias drain current), the gate is shorted to the source for the depletion type FET as described for g_m calibration. This test does not apply to enhancement type FET's. For the I_{DSS} measurement, meter M1 is shunted by 1.87-ohm resistor R11. Resistor R9, in the emitter circuit of Q2, is shorted. When power is applied to the circuit, a pulsed voltage again appears at the drain of the FET under test. However, current flows through meter M1 only when Q1 is turned on. (When Q2 conducts, no current flows thru M1.) The meter is calibrated with the shunt to read 50 ma of I_{DSS} at full scale.

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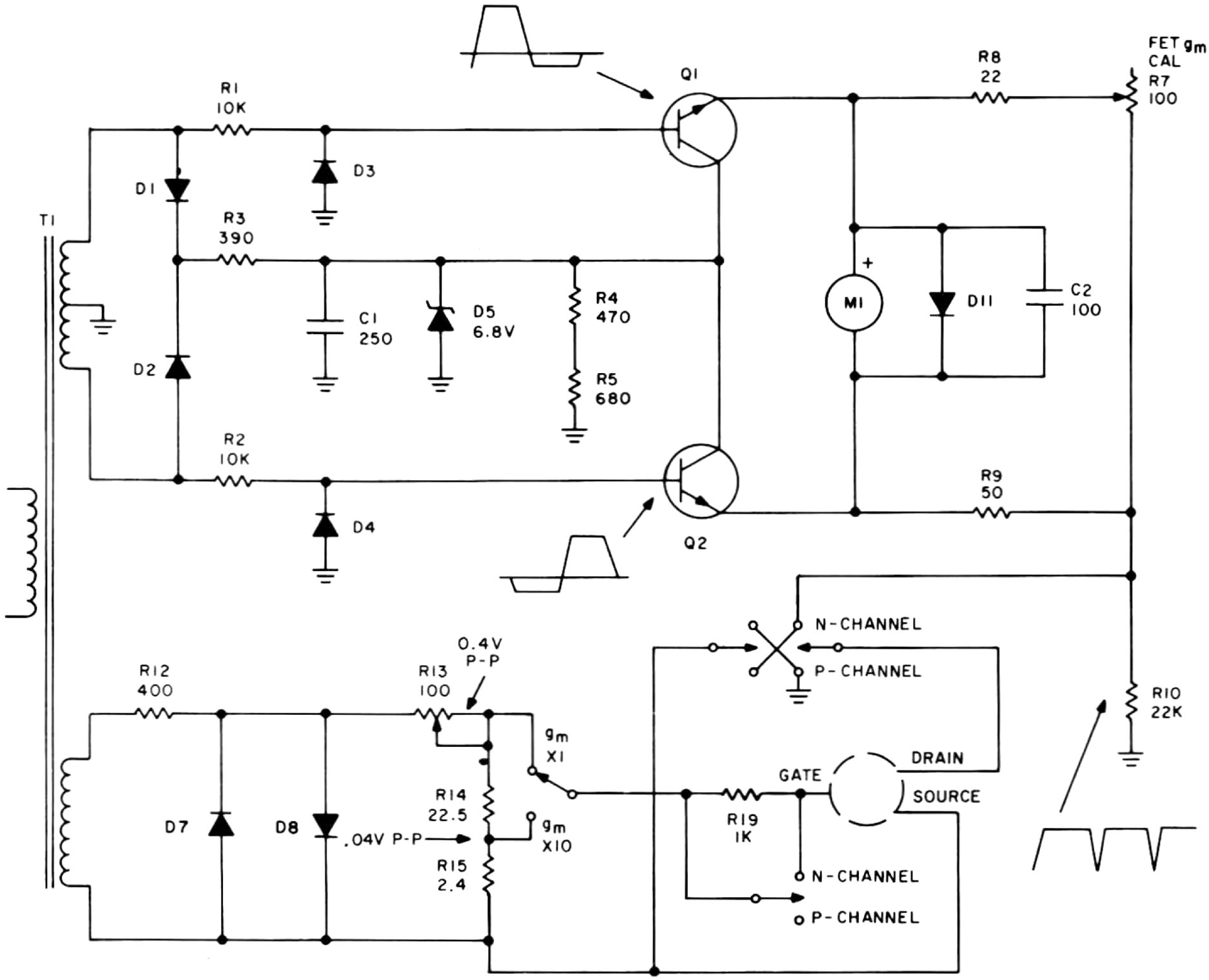

Figure 2A. g_m X1 - g_m X10 Circuit, Depletion Mode FET

e. Diode Testing.

The diode test circuit is the same as that used for measuring I_{DSS}. (See figure 3.) In this case, the diode under test rather than an FET is connected between the drain and source terminals. When the TYPE SELECTOR switch is set to the DIODE-ON source position, the anode of the diode is connected to the drain connection and the cathode to the source connection (ground terminal).

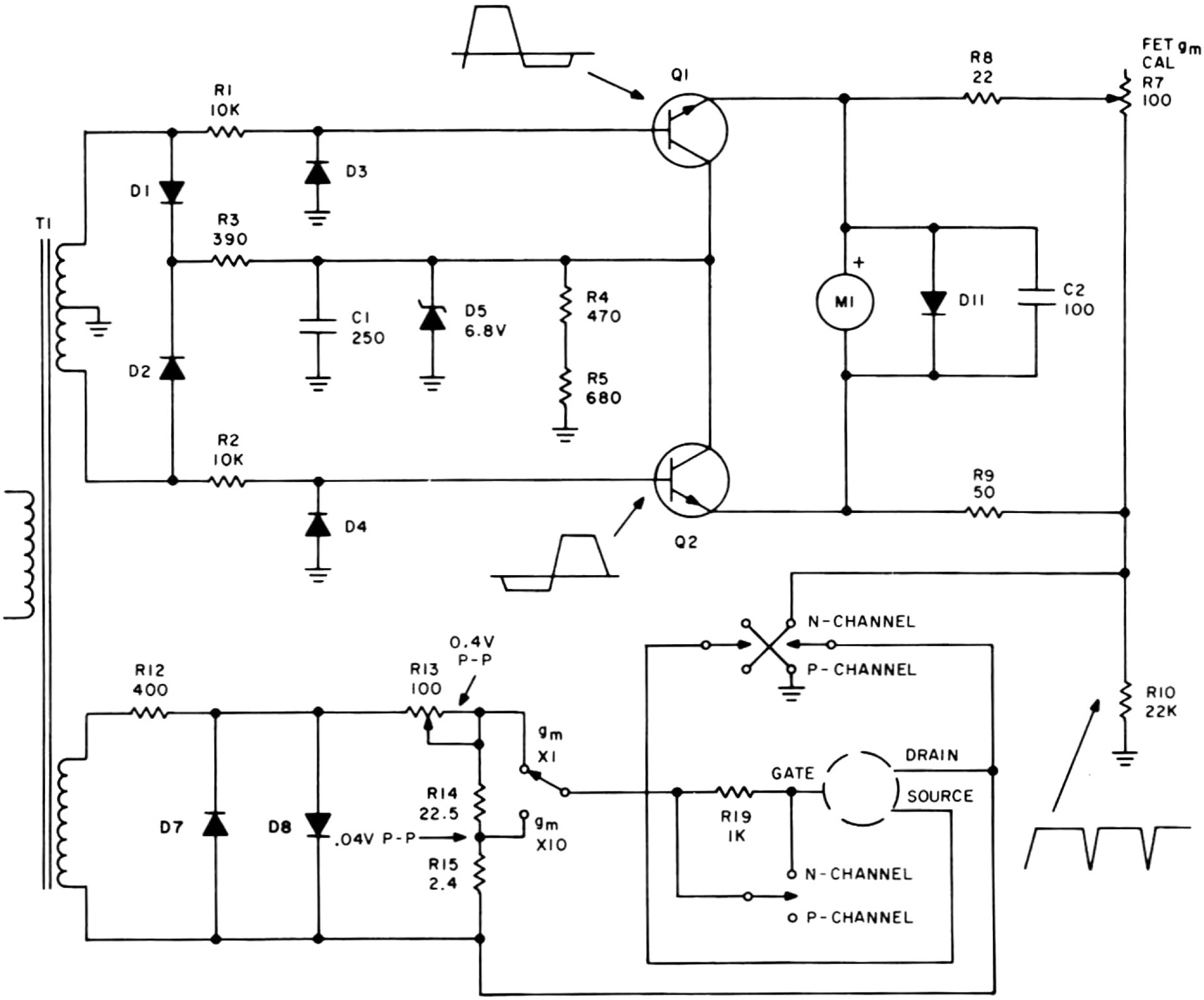

Figure 2B. g_m X1 - g_m X10 Circuit, Enhancement Mode FET

Since the diode is forward biased, current flow through the meter (a function of the Q1 collector current) is relatively high, and an up-meter deflection is produced. When the TYPE SELECTOR switch is set to the DIODE-OFF position, the diode connections are reversed, the diode is back biased, and no (or very little) meter deflection occurs. The ratio of the diode-on to diode-off meter readings is an indication of the quality of the device. Higher ratios are, of course, more desirable.

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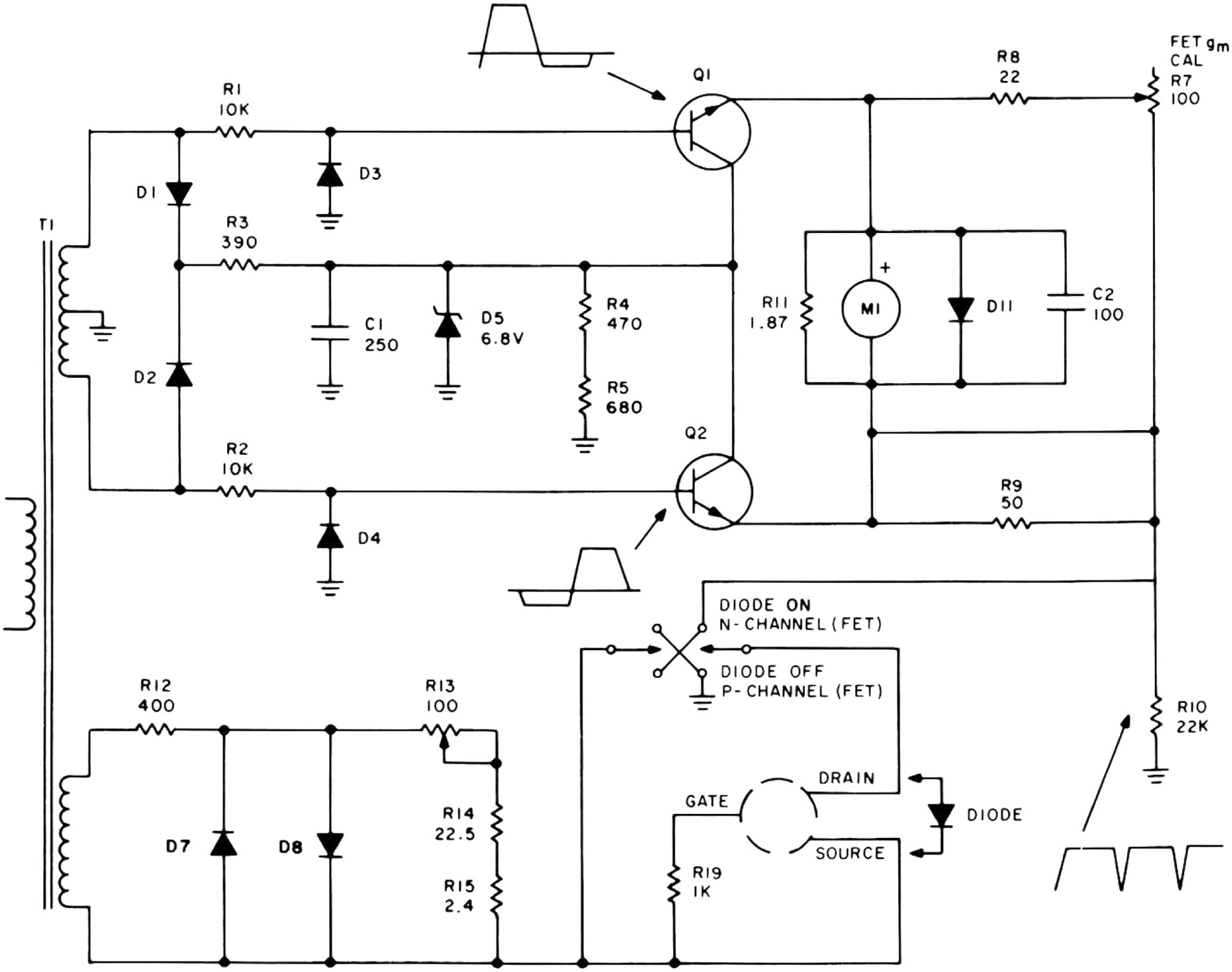
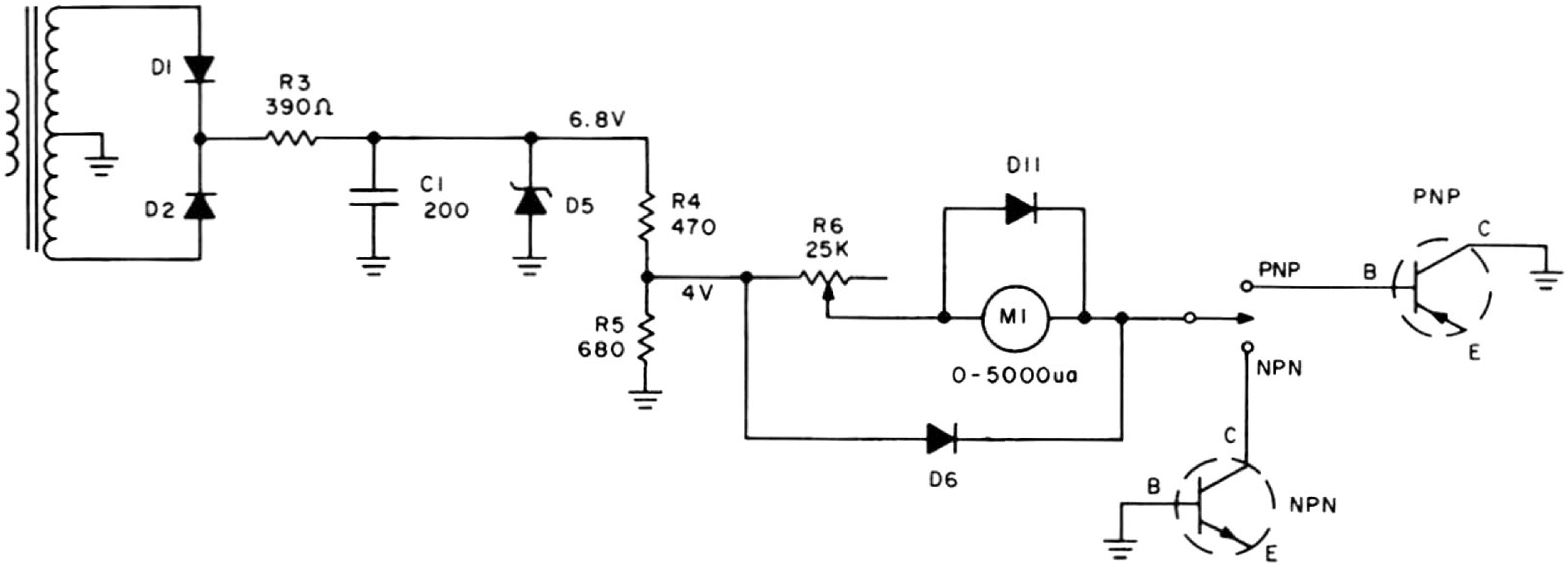


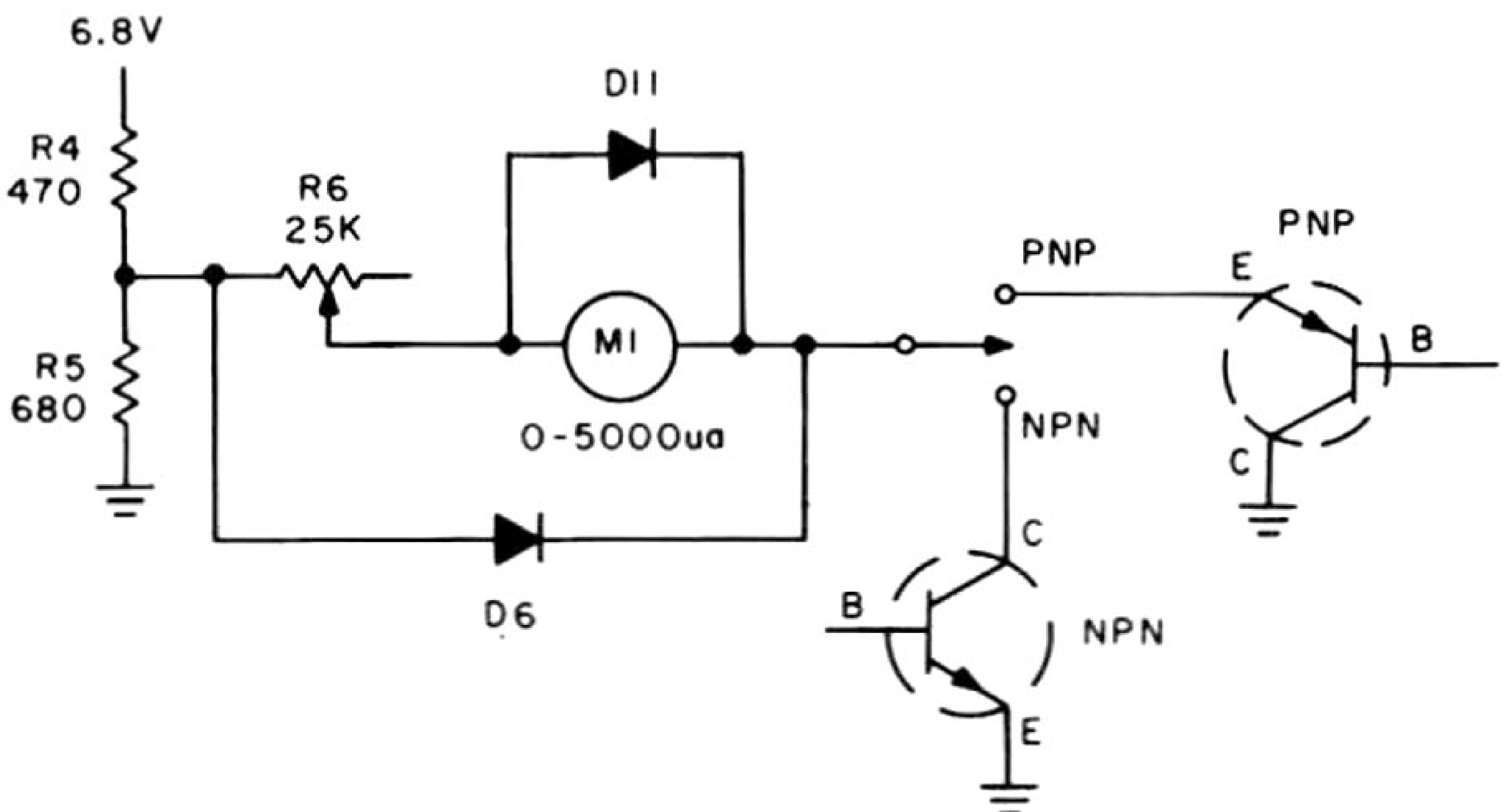
Figure 3. I_{DSS} Measurement (Depletion Only) and Diode Testing

f. Measurement of I_{CBO}.

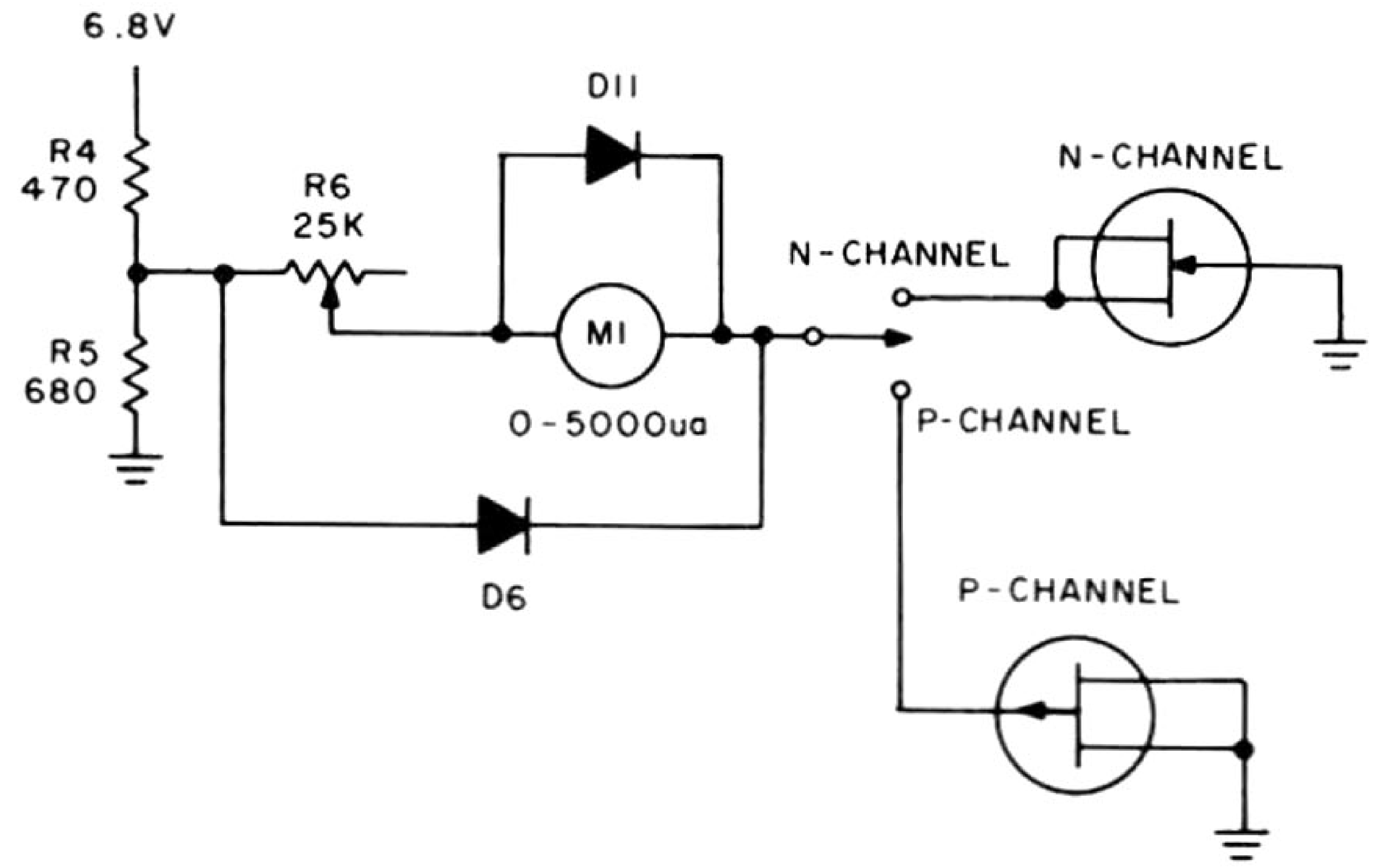
When measuring I_{CBO} in a bipolar transistor, the collector and base are connected to a metering circuit driven by a 4-volt d-c supply, as shown in figure 4A. Diode D6 shunts current around the meter circuit at higher leakage current values, effectively compressing the upper end of the 0-5000 μa leakage scale. At low leakage values, the diode opens, resulting in a linear scale at the low end of the dial. Thus, low values of leakage can be accurately read, while still permitting high-leakage measurement, all on one scale and one knob setting. The NPN or PNP setting of the TYPE SELECTOR switch determines the connections for the transistor under test.



A. I_{CBO}



B. I_{CEO}



C. I_{GSS}

Figure 4. I_{CBO}, I_{CEO}, and I_{GSS} Measurement

g. Measurement of I_{CEO} and I_{CES}.

I_{CEO} measurements are made in a similar fashion as I_{CBO}. (See figure 4B.) In this case, the base of the bipolar transistor under test is open, and the collector-emitter leakage is measured in the same d-c circuit. I_{CES} is measured using the identical circuit, but in this case the base lead of the transistor is connected to the emitter lead of the transistor.

h. Measurement of I_{GSS}.

When measuring I_{GSS} in an FET, the source and drain are shorted by the Model 685 and the same basic circuit described in "f" above, is used to measure leakage current. (See figure 4C.) The N-

CHANNEL or P-CHANNEL setting of the TYPE SELECTOR switch determines the connections required for the FET under test.

i. Measurement of V_p.

When measuring V_p, a calibrated negative voltage is fed from the arm of VOLTAGE control R18 to the gate of the FET under test. (See figure 5.) Drain current is then monitored by meter M1, which is connected in a shunt diode configuration as previously described for the leakage measurement circuits. As the arm of the control is turned up, the FET gate is driven more negative and the drain current reading on the leakage scale is reduced. When current has decreased to the pinch-off level (generally taken as 50 μa), the V_p voltage is read off the 0-20V calibrated VOLTAGE control dial.

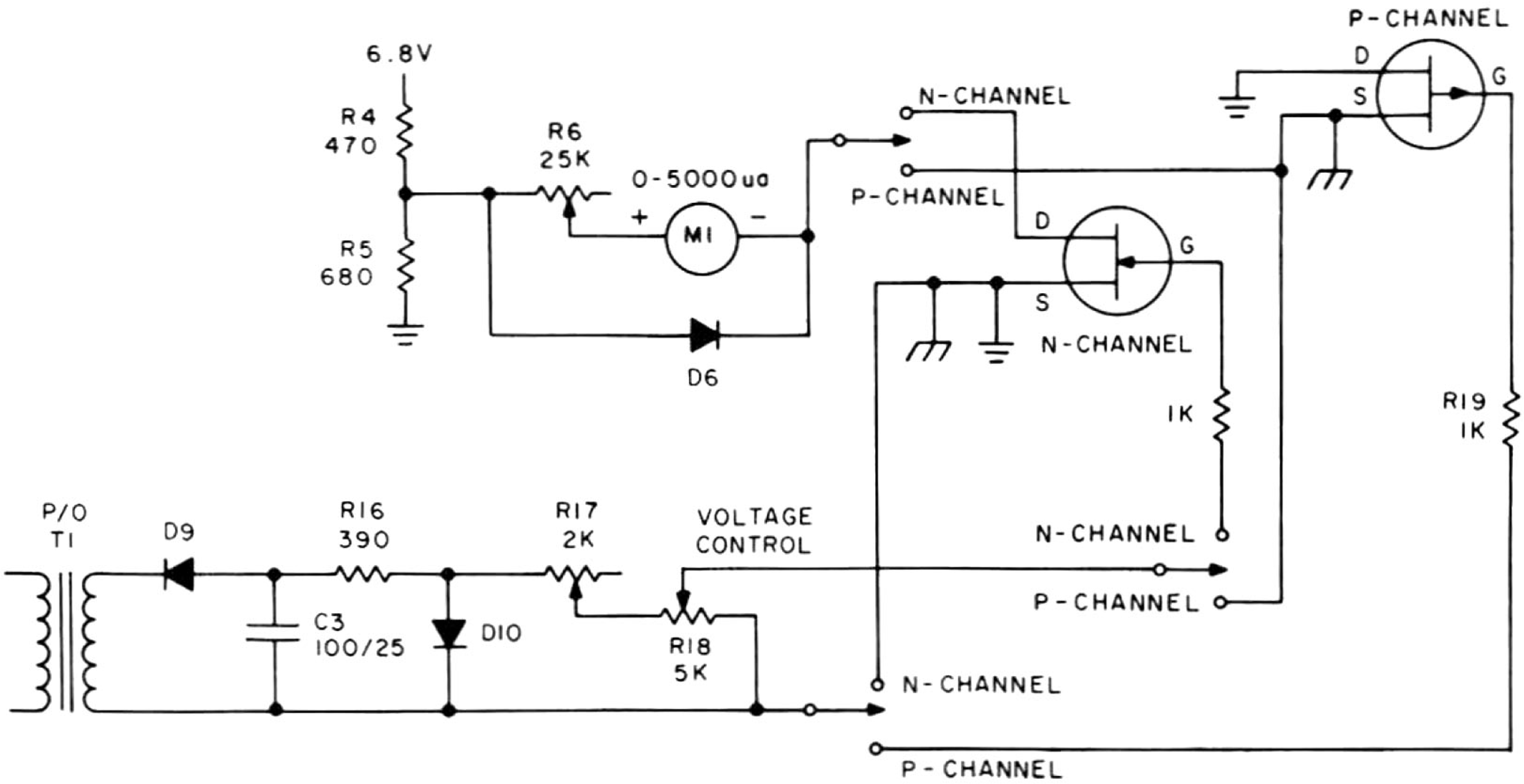


Figure 5. V_p Measurement

j. SCR and Triac Testing.

To check an SCR, it is connected as shown in figure 6. The SCR cathode is connected back to the arm of the VOLTAGE control, and the SCR gate is returned to the bottom of the control as shown. If the arm of the control is set to the low end, gate voltage is zero with respect to the cathode, and the SCR remains off. As the arm of the control is raised, the gate-to-cathode voltage rises. When the turn-on voltage level is reached, the SCR conducts, producing a deflection on the meter. On a good SCR, the device can be turned on as the voltage is increased from zero and turned off as the voltage is reduced to zero.

A Triac is connected in a like manner. The gate connection is the same as for the SCR. One anode is connected to the cathode lead and the other to the anode lead of the SCR test. In one direction of connection, the Triac will conduct, regardless of the VOLTAGE control setting. Reversing the connections to the Triac anodes will produce deflection only as the VOLTAGE control is advanced, as in the case of the SCR.

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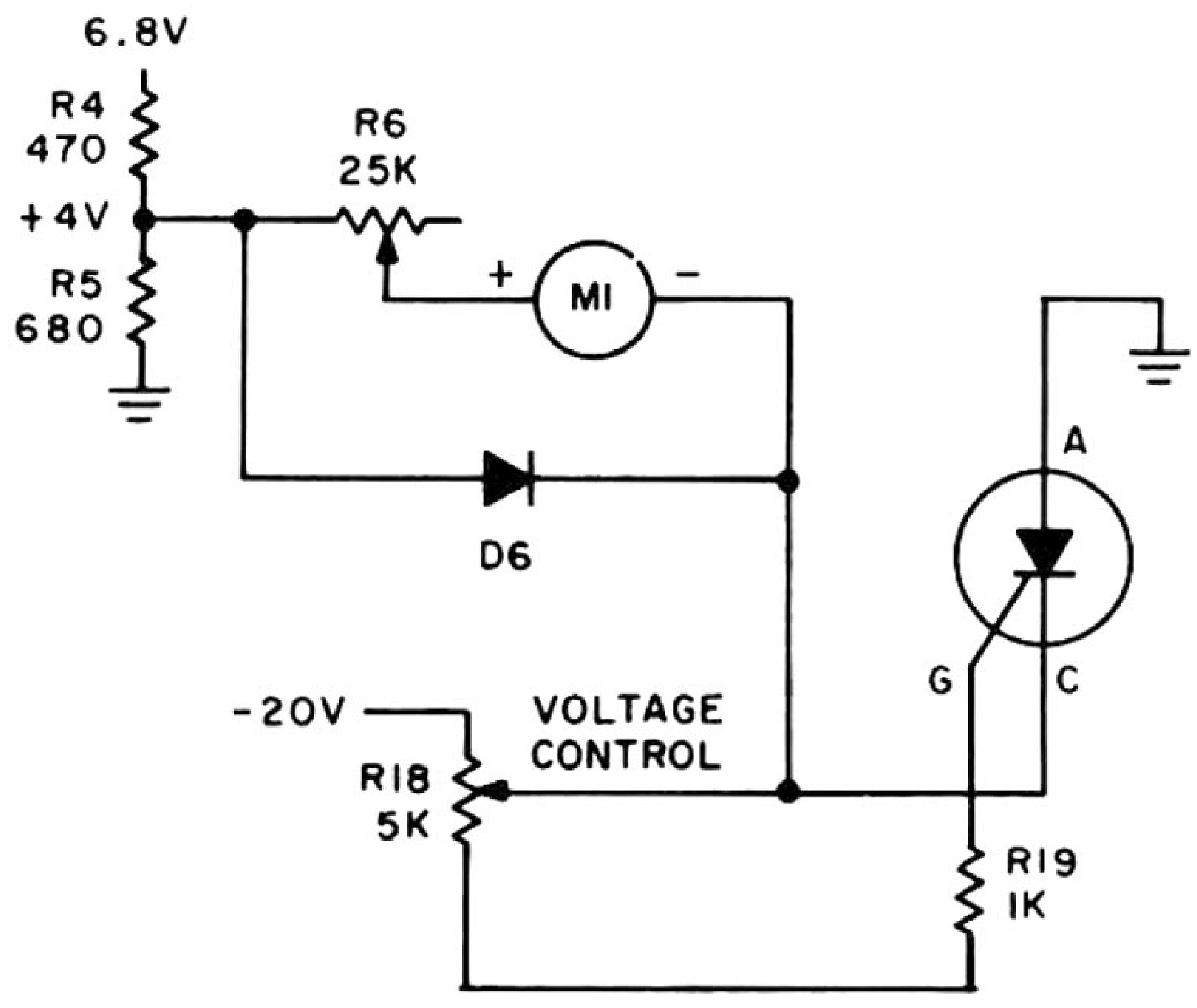


Figure 6. SCR Testing

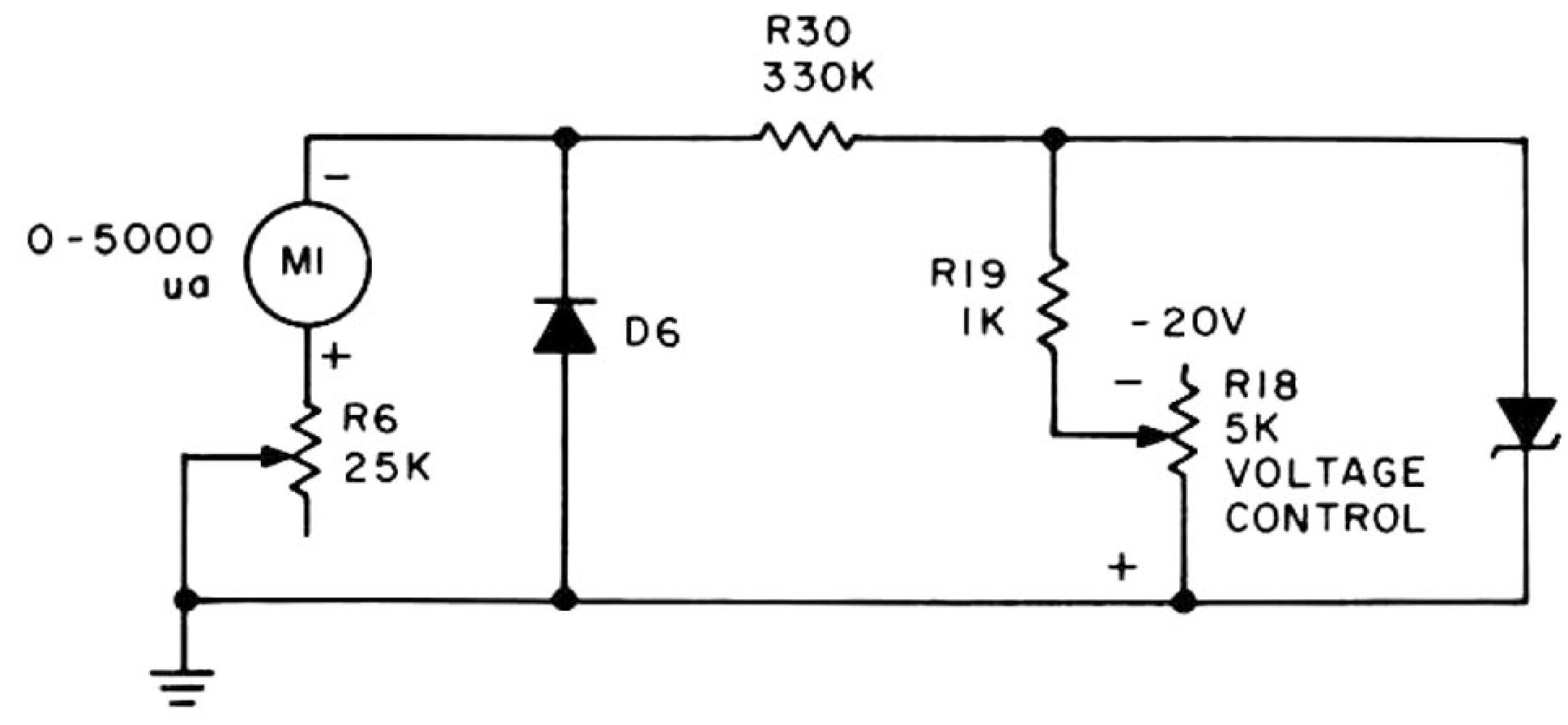


Figure 7. Zener Diode Testing

k. Zener Diode Testing.

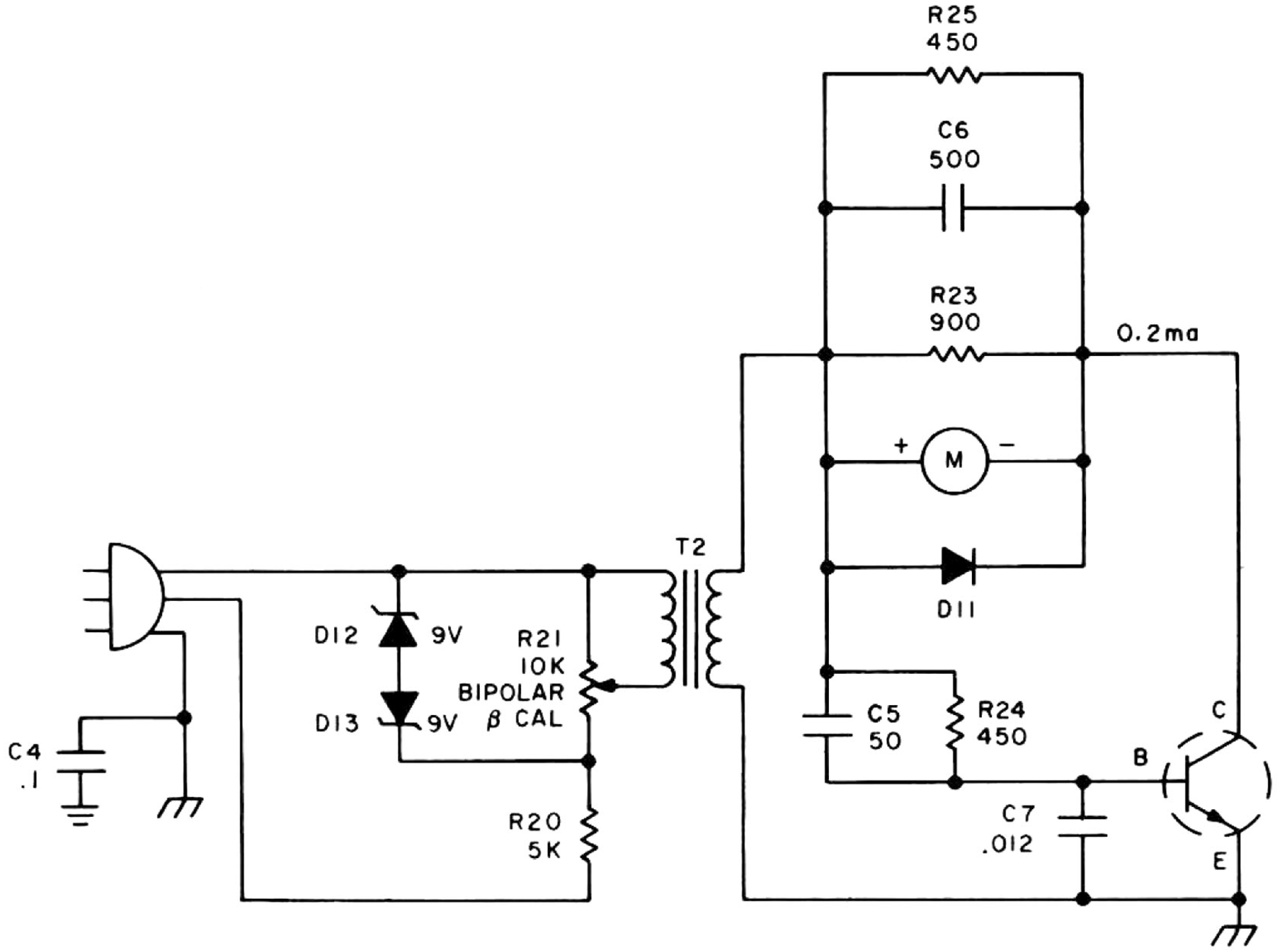
In the test circuit shown in figure 7, the zener diode under test is connected across the 0-20-volt supply. When the VOLTAGE control arm is turned up from its minimum voltage position, the meter current through R30 increases and the d-c voltage across the diode rises. When the zener breakdown voltage is reached, the diode under test conducts, limiting the voltage across the series combination of R18 and R19 to the zener voltage. Further rotation of the VOLTAGE control arm does not increase the voltage across R18 and R19 and the meter reading does not change. The zener breakdown voltage can then be read off the VOLTAGE control dial as the lowest voltage reading that will not permit the meter to deflect further.

l. Measuring β in Bipolar Transistors.

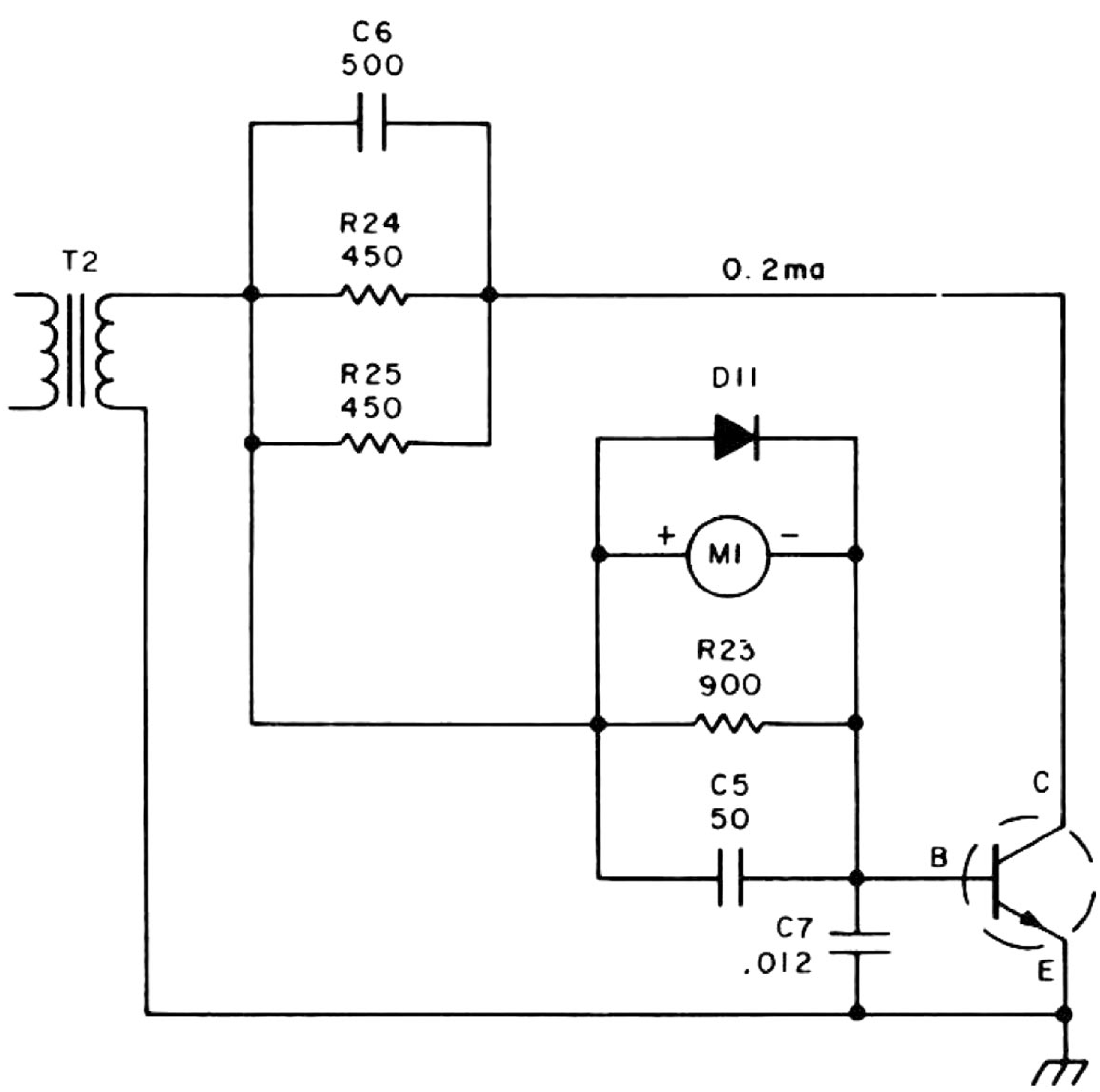
Transformer T2 supplies the voltages necessary to measure a-c beta (β) in bipolar transistors. In the r-f transistor test circuit of figure 8A, diodes D12 and D13 clip the a-c voltage developed across the BIPOLAR β CAL control so that a square wave of fixed voltage is impressed across the primary of T2. This control sets the a-c input to T2 to a level that produces 0.2 ma of average collector current in the transistor under test. The meter shunt resistors are designed to provide full-scale deflection (corresponding to β = 2 on the Model 685) at 0.2 ma of collector current. (The circuit shown applies to NPN transistors; the PNP test circuit is similar, with meter polarity reversed.)

When the PUSH TO READ β switch is held down, the meter is transferred to the base circuit of the transistor to measure the average base current. (See figure 8B.) Since $\beta = \frac{\Delta I_C}{\Delta I_B}$ and I_C is maintained constant at 0.2 ma, β is proportional to $\frac{1}{\Delta I_B}$ and the meter is calibrated against the average base current reading. The β scale on the Model 685 is calibrated downward rather than upward because of the reciprocal function.

A similar circuit is used to measure β of signal transistors. (See figure 9.) In the SIG β X1 position of the BIPOLAR FUNCTION switch, the BIPOLAR β CAL control is adjusted for an average collector current of 2 ma. Operation of the β measuring circuit is the same as that described for the RF β X1 position of the BIPOLAR FUNCTION switch.

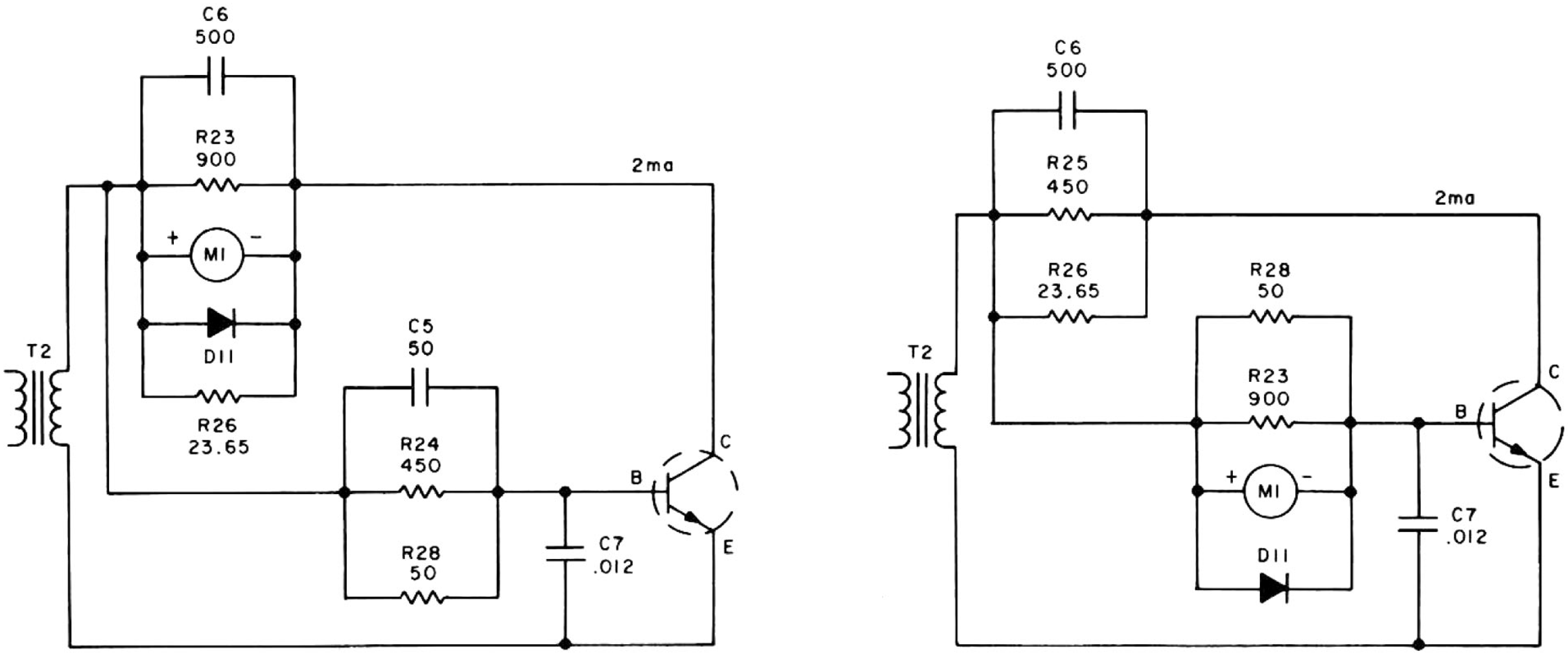


A. CALIBRATION CIRCUIT



B. TEST CIRCUIT

Figure 8. RF Transistor Testing

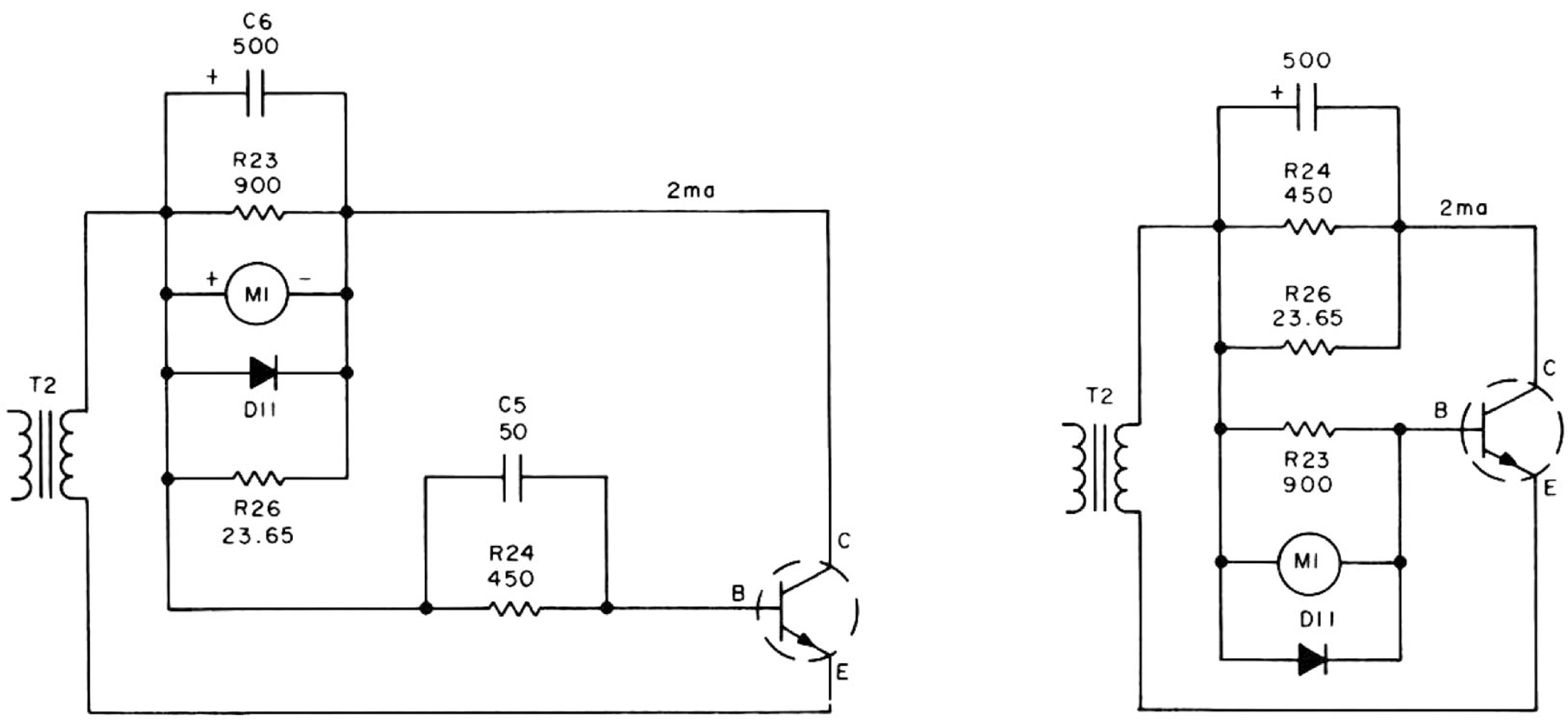


A. CALIBRATION CIRCUIT

B. TEST CIRCUIT

Figure 9. SIG β X1 Transistor Testing

In the SIG X10 position, the resistance in the base circuit is increased to 10 times its original value (from 45 ohms to 450 ohms) so that the same full-scale deflection of 2 ma (now corresponding to β = 20 on the Model 685) is produced by 1/10 the base current. (See figure 10.) In effect, the metering circuit is now 10 times more sensitive, measuring β values from 20 to 1000, with readings to 10,000.



A. CALIBRATION CIRCUIT

B. TEST CIRCUIT

Figure 10. SIG β X10 Transistor Testing

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When using the PWR β X1 position of the BIPOLAR FUNCTION switch, full-scale meter deflection is produced by 20 ma of collector current. (See figure 11.) As in the other β positions, the meter is switched to the base circuit to measure the β of power transistors.

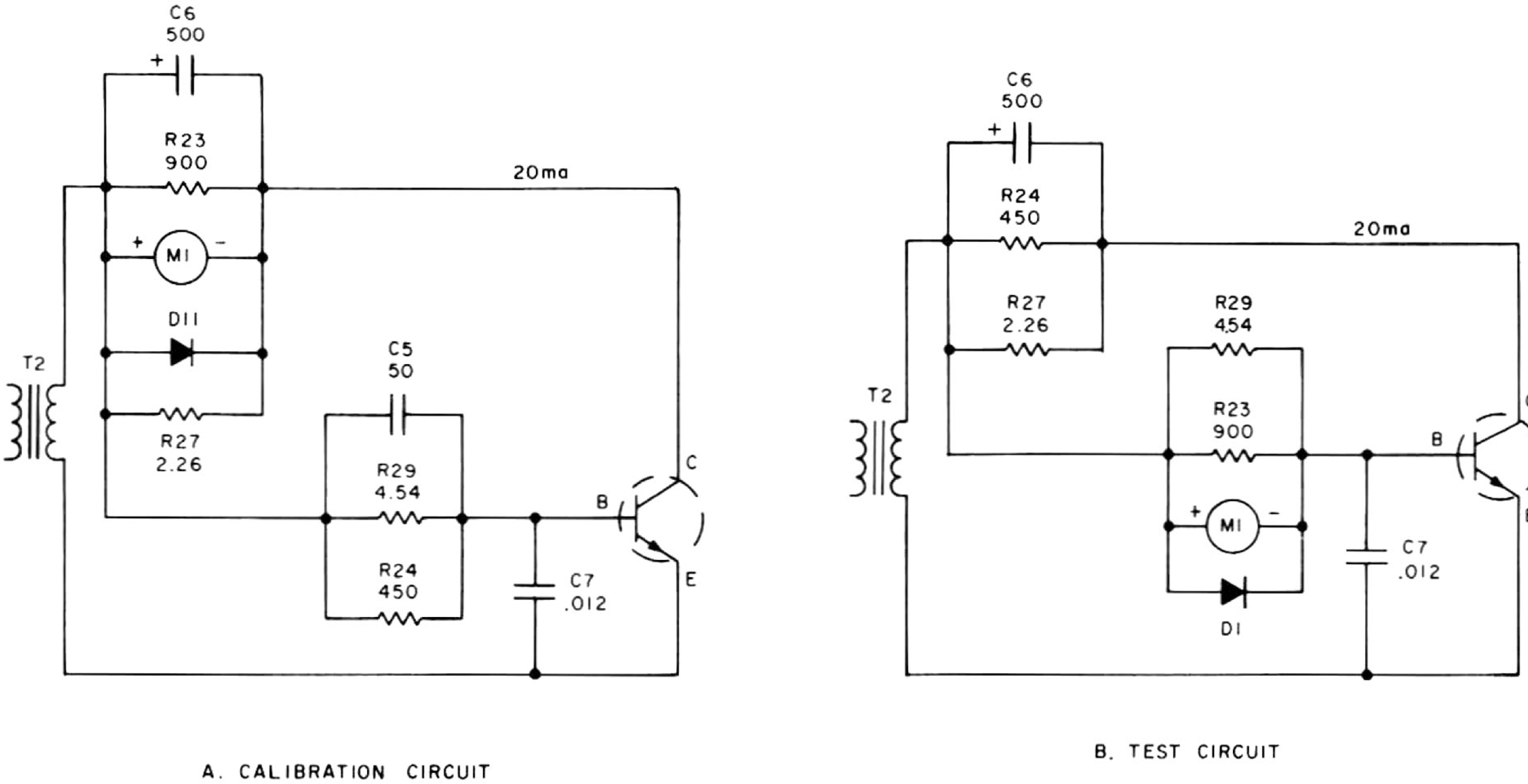


Figure 11. PWR β X1 Transistor Testing

In the PWR β X10 position, the base resistance is again made 10 times its previous value, permitting β values between 20 and 1000 to be measured, with readings to 10,000. (See figure 12.)

m. Ohmmeter Operation.

The ohmmeter circuit also makes use of the diode-controlled compressed scale circuit. (See figure 13.) The VOLTS/OHMS terminals can be used to measure resistance values ranging from 400 ohms to 10 megohms, all on one scale and at the same knob setting.

n. Voltmeter Operation.

In voltmeter operation, d-c power is removed from the metering circuit. (See figure 14.) Multiplier resistor R30 permits measurement up to 500 volts. Again, the compressed scale provides a linear calibration at lower voltages (normally used in transistor circuits), while permitting higher voltage measurements on the compressed end of the scale. All readings are made while using only one knob setting.

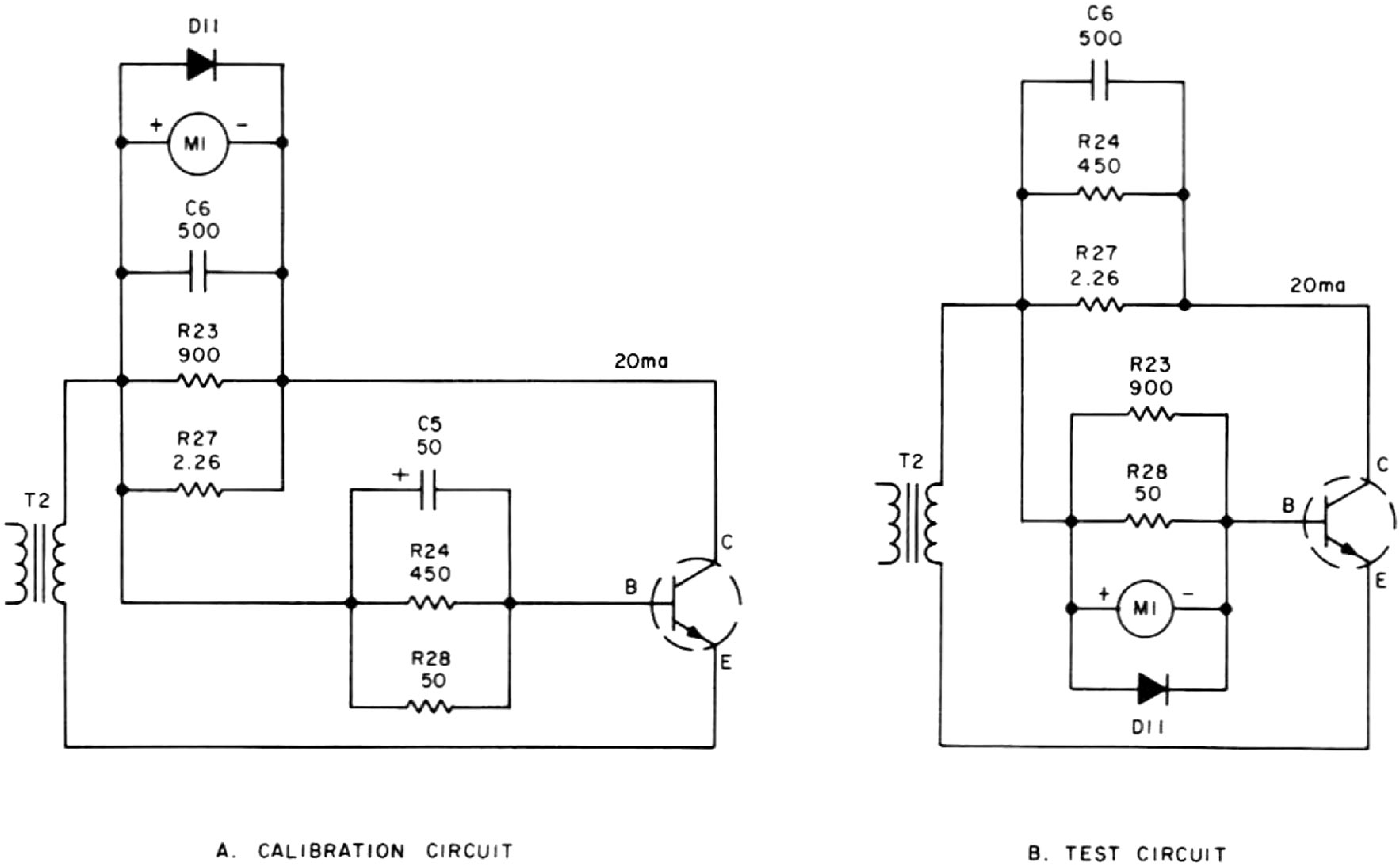


Figure 12. PWR β X10 Transistor Testing

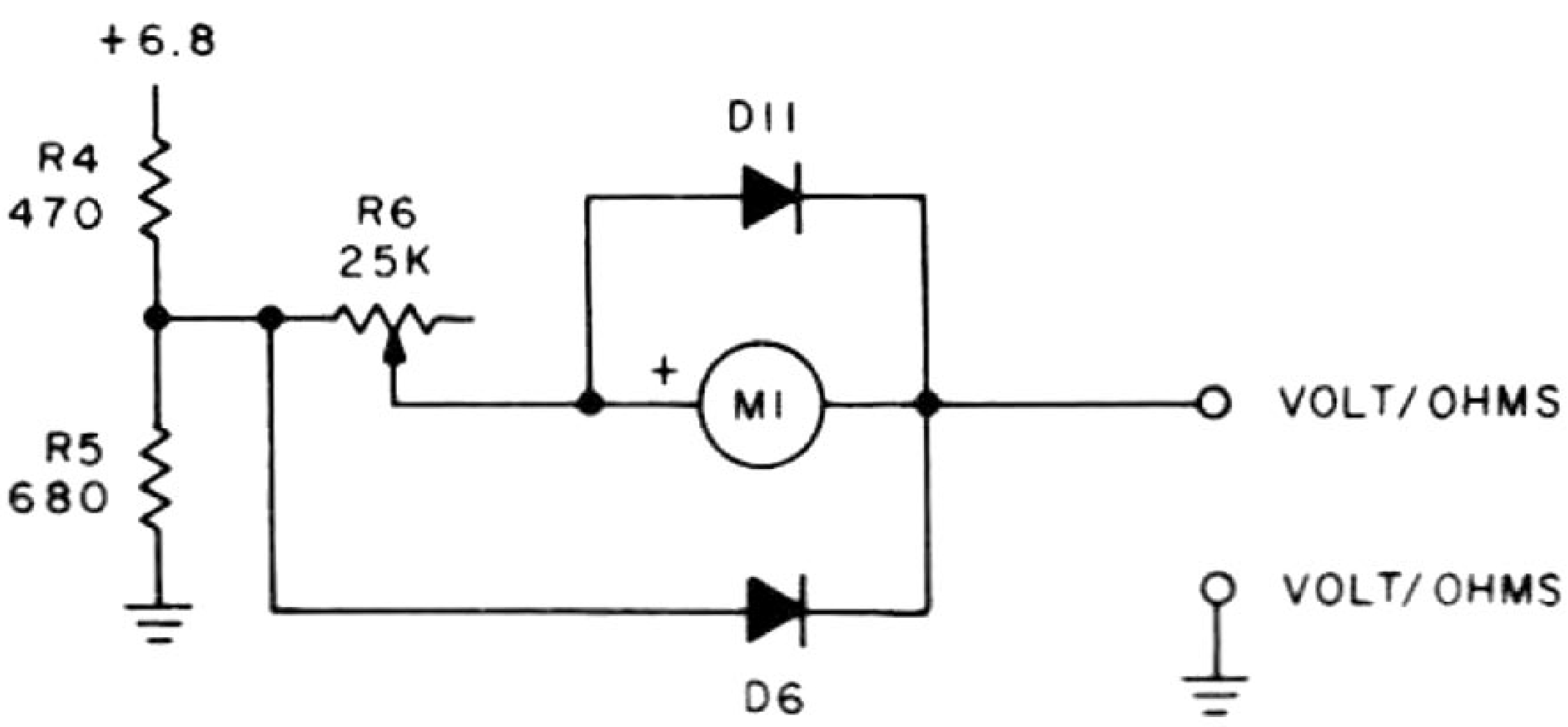


Figure 13. Ohmmeter Circuit

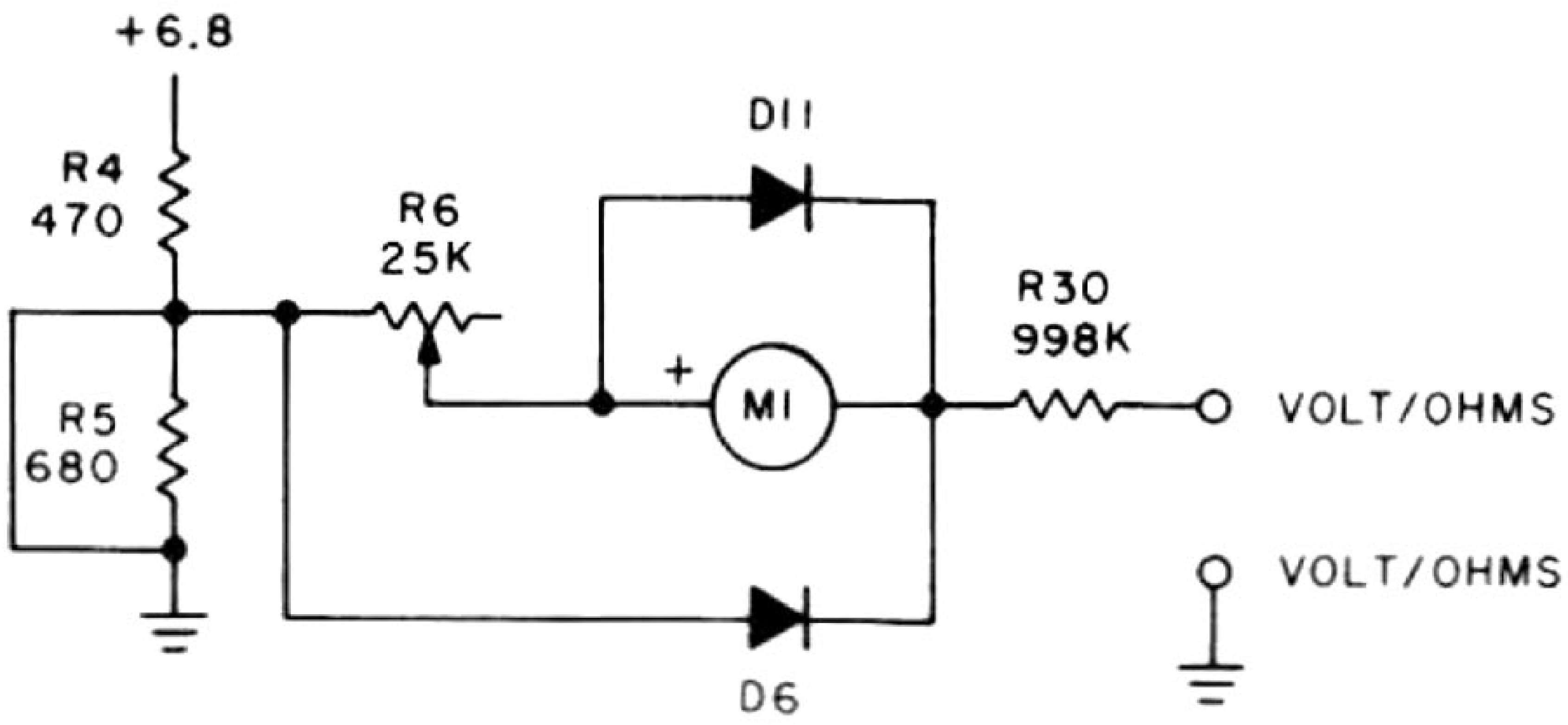
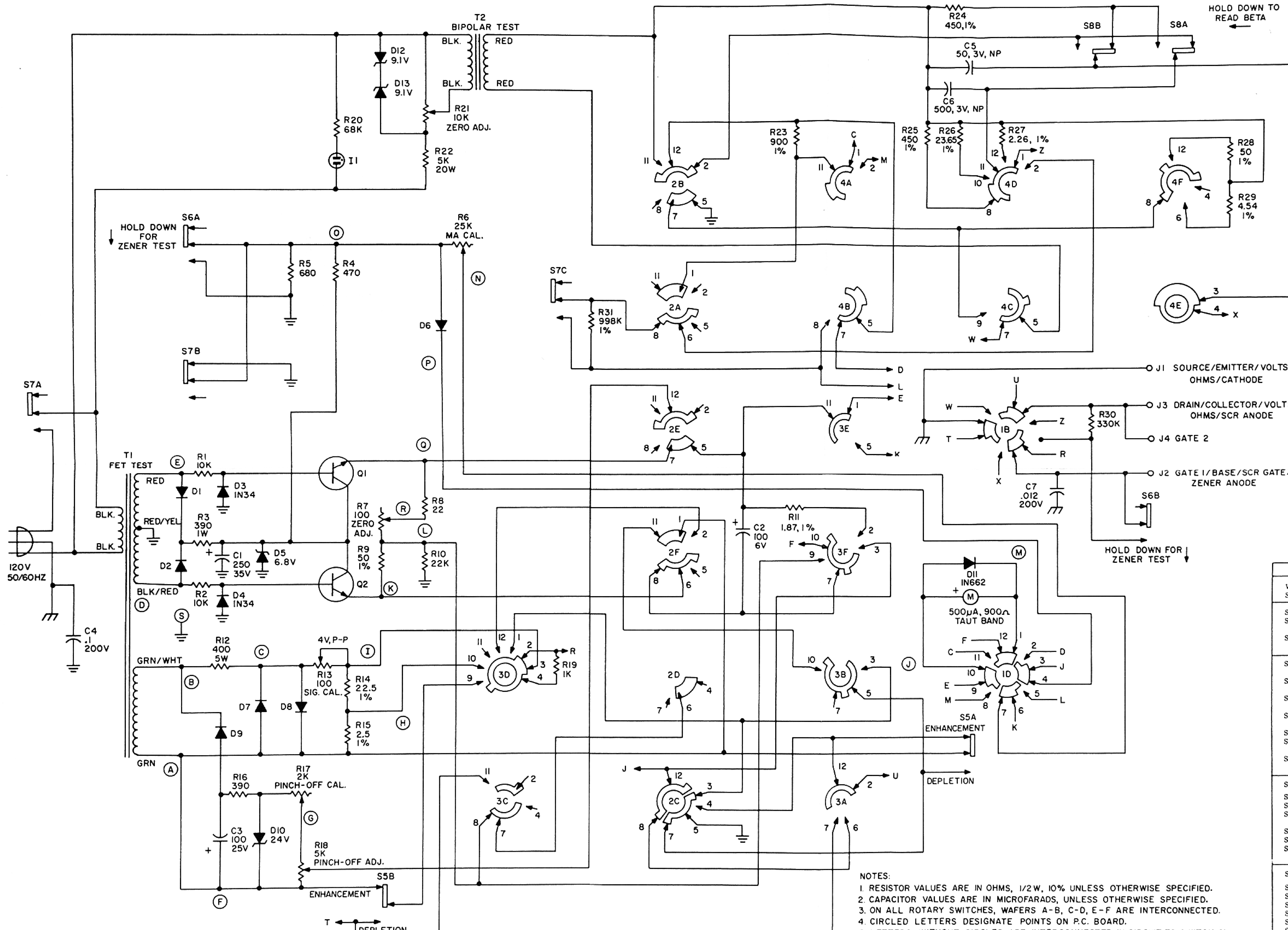


Figure 14. Voltmeter Circuit



NOTES:
1. RESISTOR VALUES ARE IN OHMS, 1/2W, 10% UNLESS OTHERWISE SPECIFIED.
2. CAPACITOR VALUES ARE IN MICROFARADS, UNLESS OTHERWISE SPECIFIED.
3. ON ALL ROTARY SWITCHES, WAFERS A-B, C-D, E-F ARE INTERCONNECTED.
4. CIRCLED LETTERS DESIGNATE POINTS ON P.C. BOARD.
5. LETTERS WITHOUT CIRCLES ARE INTERCONNECTED IN CIRCUIT TO SWITCH S1.

S1 - ROTARY SWITCH

POS. 1 - FET/UJT/DIODE/SCR/ZENER
POS. 2 - BIPOLAR/VOLTS/OHMS

S2 - ROTARY SWITCH

POS. 1 - N-CH/NPN/OHMS/DIODE ON/ZENER
POS. 2 - P-CH/PNP/VOLTS/DIODE OFF/SCR

S3 - ROTARY SWITCH

POS. 1 - g_m X1
POS. 2 - g_m CAL
POS. 3 - g_m X10
POS. 4 - I_{DSS}/DIODE
POS. 5 - V_p/SCR/ZENER
POS. 6 - I_{GSS}/UJT

S4 - ROTARY SWITCH

POS. 1 - RF X1
POS 2 - SIG X1
POS 3 - SIG X 10
POS. 4 - PWR X 1
POS. 5 - PWR X10
POS. 6 - I_{CBO}
POS 7 - I_{CEO}/VOLTS/OHMS

S5 - SLIDE SWITCH

POS. 1 - ENHANCEMENT
POS. 2 - DEPLETION

S6 - SLIDE-SPRING RETURN SWITCH

PUSH FOR ZENER TEST

S7 - SLIDE SWITCH

POS. 1 - VOLTS/POWER OFF
POS. 2 - POWER ON

S8 - SLIDE-SPRING RETURN SWITCH

PUSH TO READ BETA

WAFER SURFACE	POSITIONS 1	2	3	4	5	6	7
S1	FET	BIPOLAR					
S1B	1-2 5-6 9-10	2-3 6-7 10-11					
S1D	1-12 3-4 6-7 9-10	1-2 4-5 7-8 10-11					
S2	N-CH/ NPN	P-CH/ PNP					
S2A	1-11 6-8	1-2 5-6					
S2B	2-12 5-7	7-8 11-12					
S2C	3-5-7 8-12	3-12 4-5-8					
S2D	4-6	6-7					
S2E	2-12 5-7	7-8 11-12					
S2F	1-11 6-8	1-2 5-6					
S3	g_m X1	g_m CAL	G_m X10	I_{DSS}	V_p	I_{GSS}	
S3A	2-12	2-12	2-12	2-12	2-6	2-6-7	
S3B	5-7	5-7	5-7	5-7	3-7-10		
S3C	7-8	7-8	2-3 7-8	7-8			
S3D	2-3-4	3-4-9	4-10	4-11	4-12	4-1	
S3E	1-11	1-11	1-11	1-11	1-5	1-5	
S3F	7-10	7-10	7-10	2-7-9- 10	3-10	3-10	
S4	RF X1	SIG X1	SIG X10	PWR X1	PWR X10	I_{CBO}	I_{CEO}
S4A	1-11	1-11	1-11	1-11	1-11	1-2	1-2
S4B	5-7	5-7	5-7	5-7	5-7	5-8	5-8
S4C	5-7	5-7	5-7	5-7	5-7		7-9
S4D	1-8-11	1-10-11	1-10-11	1-11-12	1-11-12	1-2	1-2
S4E	3-4	3-4	3-4	3-4	3-4	3-4	
S4F		4-12		4-6	4-12	4-8	

EICO 685 SCHEMATIC DIAGRAM

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